COSC 121
Spring 2019
Assignment 7
Due April 11, 2019

This assignment relates to the 5-stage pipeline in Chapter 4 of [PH]. For timelines, it is recommended that you use the format illustrated below.

add $1, $2, $3	IF	ID/RF	EX	MEM	WB				
or …		IF	ID/RF	EX	MEM	WB			
lw …			IF	stall	stall	stall	ID/RF	MEM	EX

"stall" in the figure above is shown as "bubble" in the figures in [PH]. It denotes that the instruction stalls for 1 cycle waiting for a hazard to be resolved.

Consider the following assembly program. The comments explain the functionality of instructions in the program.

```
add    $1, $2, $3      ; add contents of registers 2 and 3, store result in register 4
add    $2, $1, $4
add    $5, $6, $7
or     $8, $9, $0      ; bitwise OR of contents of registers 9 and 0 is stored in register 8
```

1. How many cycles will be required to complete the program above if instruction execution **stalls** to resolve data hazards? Explain your answer using a timeline of the execution of the instructions.

2. In this question (similar to Question 1), assume that instruction execution **stalls** to resolve data hazards. It is possible to reorder the instructions above without changing the outcome of the program, such that the total number of cycles required to perform the instructions will be smaller than that in Question 1.

   Show a reordering of the above instructions such that the total number of cycles required will be minimized.

3. Suppose that we **do not** want to use any special-purpose hardware or any mechanisms to detect data hazards in our pipeline. Suppose that the "nop" instruction does not perform any operation at all.

   Show a modified version of the above code, inserting "nop" where useful, such that the code will execute correctly (i.e., data hazards will not affect correctness of the outcome) despite the lack of mechanisms for detecting data hazards.

4. Suppose that **data forwarding** is utilized to improve performance when data hazards occur. For the program shown above, how many cycles will be required in this case? Explain your answer using a timeline.

5. Suppose that register $1 contains 10, and register $0 contains 0, immediately before the program below is executed.

```
Loop:  addi   $1, $1, -1      ; add -1 to register 1 and store result in register 1
                              ; the above add decrements register 1 by 1
                              ; "addi" denotes "add immediate"
       nop                    ; no-op
       nop
       nop
       bne    $1, $0, Loop    ; "branch if not equal"
                              ; if register 1 is not equal to register 0, branch to Loop
```

   Until it is known whether a branch is taken or not, the pipeline executes the instructions that follow the branch sequentially.

   Assume that when a branch is taken, the target instruction is fetched in cycle 5 of the branch (i.e., when the branch is in the WB stage, the target instruction is in the IF stage) – thus, when a branch is taken, the three instructions (which follow the branch sequentially) in the IF, ID/RF and EX stages of the pipeline are *flushed* (or discarded).

   Estimate the total number of cycles required to execute the above code. Briefly explain your answer.

SUGGESTED EXERCISE:

Re-do questions 1 through 4 for other programs with data hazards. For instance, add one more instruction before the first instruction, namely,

```
lw     $2,  $0(5)      ; load into register 2 the contents of memory location $0 + 5
```